

1 2. The output driver of claim 1 wherein the first drive
2 block is connected in parallel with the second drive block.

1 3. The output driver of claim 1 wherein the first drive
2 block includes one or more first drive transistors, the second
3 drive block includes one or more second drive transistors,
4 the first and second drive blocks having the same number of
5 drive transistors, wherein the first drive transistors of the
6 first drive block provide twice as much current as the second
7 drive transistors of the second drive block.

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1 4. (Amended) The output driver of claim 1 wherein the first
2 drive block includes [one] two or more first drive
3 transistors, the first drive transistors being binary weighted
4 with respect to each other to provide correspondingly weighted
5 amounts of current in response to the MSB, the second drive
6 block includes [one] two or more second drive transistors, the
7 second drive transistors being binary weighted with respect to
8 each other to provide correspondingly weighted amounts of
9 current in response to the LSB, the first and second drive
10 blocks having the same number of drive transistors.

1 5. The output driver of claim 3 wherein a set of current
2 control signals enables and disables corresponding ones of the
3 first and second drive transistors.

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1 6. (Amended) The output driver of claim 1 wherein binary
2 signaling is used by setting the LSB [symbol] equal to zero.

1 7. The output driver of claim 3 wherein drive transistors
2 are connected to an I/O pin,
3 further comprising at least one constant current transistor
4 connected to the I/O pin to provide a substantially
5 continuous flow of current through the I/O pin to increase
6 noise immunity.

1 8. An output driver to drive an output symbol representing
2 two or more bits including a most significant bit (MSB) and a
3 least significant bit (LSB), comprising:

4 a logic circuit to generate a set of transistor enable
5 signals based on a state of the MSB and the LSB; and

6 a set of weighted transistors, each weighted transistor
7 being responsive to one transistor enable signal of the set of
8 transistor enable signals.

1 9. The output driver of claim 8 wherein the weighted
2 transistors of the set of weighted transistors are weighted
3 to compensate for gds distortion.

1 10. The output driver of claim 8 further comprising:
2 a set of current control transistors, responsive to
3 current control signals, coupled to the set of weighted
4 transistors, to adjust an amount of current supplied by the
5 output driver.

1 11. (Amended) The output driver of claim 8 [wherein each
2 weighted transistor is differentially coupled to another
3 correspondingly weighted transistor that is enabled to provide
4 a continuous flow of current to increase noise immunity]
5 further comprising at least one current source coupled to
6 at least one weighted transistor to provide a substantially
7 continuous flow of current to reduce switching noise.

1 12. (Amended) An output driver to drive an output symbol
2 representing two or more bits including a most significant bit
3 (MSB) and a least significant bit (LSB), comprising:
4 a logic circuit to generate a set of transistor enable
5 signals in accordance with a state of the MSB and LSB; and
6 a set of drive blocks, each drive block being responsive
7 to one of the transistor enable signals, each drive block
8 including a drive transistor responsive to one of the

9 transistor enable signals, at least a [of] subset of the drive
10 blocks including a gds compensation transistor [resposive]
11 responsive to one of the transistor enable signals, each gds
12 compensation transistor having a predefined geometry to
13 compensate for gds distortion.

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1 13. (Amended) An output driver to drive an output symbol
2 representing two or more bits including a most significant bit
3 (MSB) and a least significant bit (LSB), comprising:
4 a logic circuit to generate a set of transistor enable
5 signals in accordance with a state of the MSB and LSB; and
6 a set of drive blocks, each drive block including a set
7 of drive transistors connected in series with a set of
8 current-control transistors, the drive [transistors]
9 transistors being responsive to one of the transistor enable
10 signals, the set of current-control transistors being
11 responsive to a set of current control signals, at least a
12 [of] subset of the drive blocks including a set of gds
13 compensation transistors connected in series with a set of
14 gds-current-control transistors, the gds compensation
15 transistors being [resposive] responsive to one of the
16 transistor enable signals, and the gds-current-control
17 transistors being responsive to gds-current-control signals.

1 14. The output driver of claim 13 wherein each set of drive
2 transistors of the drive block are binary weighted.

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1 15. (Amended) A bus receiver to receive an input symbol
2 representing two or more bits including a most significant bit
3 (MSB) and a least significant bit (LSB), comprising:
4 a MSB latching comparator to compare the input symbol to
5 a MSB threshold voltage to generate a first binary output
6 signal representing a state of the MSB;
7 a first LSB latching comparator to compare the input
8 symbol to a first reference voltage to generate a second

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9 binary output signal representing [the] a relationship between
10 the input symbol and the first reference voltage;
11 a second LSB latching comparator to compare the input
12 symbol to a second reference voltage to generate a third
13 binary output signal representing [the] a relationship between
14 the input symbol and the second reference voltage; and
15 a logic block to generate a fourth binary output signal
16 representing a state of the LSB in accordance with the first,
17 second and third binary output signals.

1 16. The bus receiver of claim 15 wherein the first, second
2 and third latching comparators generate their respective
3 binary output signals synchronized to a clock signal.

1 17. A bus receiver to receive an input symbol representing
2 two or more bits, each bit being associated with at least one
3 threshold voltage of a set of threshold voltages, comprising:
4 a most-significant-bit (MSB) receiver to receive the
5 input symbol and provide an MSB logic signal representing a
6 most-significant bit of the input symbol; and
7 a least-significant-bit (LSB) receiver to receive the
8 input symbol and provide an LSB logic signal representing a
9 least-significant bit of the input symbol.

1 18. The bus receiver of claim 17 wherein the MSB receiver and
2 LSB receiver include:

3 at least one integrator to generate integration voltages
4 on integration nodes by integrating charge in accordance with
5 a voltage associated with the input symbol and one or more
6 threshold voltages of the set of threshold voltages; and

7 at least one sense amplifier to receive the integration
8 voltages of the at least one integrator to generate the logic
9 signal of the respective receiver.

95 1 19. (Amended) The bus receiver of claim 17 wherein the MSB
2 receiver and LSB receiver include:

3 at least one preamplifier to generate the input symbol by
4 adjusting an unconditioned input symbol in accordance with
5 [the] a relationship of the unconditioned input symbol to
6 ranges of voltages defined by the voltages of the set of
7 threshold voltages;

8 at least one integrator to generate integration voltages
9 on integration nodes by integrating a charge in accordance
10 with a voltage associated with the input symbol; and

11 at least one sense amplifier to receive the integration
12 voltages of the at least one integrator to generate at least
13 one logic signal representing a relationship of the input
14 symbol to the one or more threshold voltages of the set of
15 threshold voltages.

1 20. (Amended) A memory comprising:

2 an array of memory cells;

3 an address decoder;

4 a plurality of bus receivers to receive an address and
5 also to receive input symbols, each input symbol representing
6 a predetermined number of bits, each bit being associated with
7 a range of voltage levels, a set of threshold voltages
8 defining each range of voltage levels, comprising:

9 a most-significant bit (MSB) receiver to determine a MSB
10 of the input symbol in accordance with a first threshold
11 voltage of the set of threshold voltages; [and]

12 a least-significant bit (LSB) receiver to determine a LSB
13 of the input symbol in accordance with second and third
14 threshold voltages of the set of threshold voltages; and

15 an I/O circuit to store the MSB of the input symbol and
16 LSB of the input symbol in a subset of memory cells of the
17 array of memory cells.

1 21. The memory of claim 20 wherein the first threshold
2 voltage is less than the second threshold voltage, and the
3 first threshold voltage is greater than the third threshold
4 voltage.

1 22. (Amended) The memory of claim 20,
2 wherein the MSB receiver includes:

3 at least one MSB integrator to generate integration
4 voltages on integration nodes by integrating charge in
5 accordance with a voltage of the input symbol with respect to
6 the first threshold voltage; and

7 at least one MSB sense amplifier to receive the
8 integration voltages of the at least one MSB integrator to
9 generate at least one MSB logic signal representing [the] a
10 relationship of the input symbol to the first threshold
11 voltage; and

12 wherein the LSB receiver includes:

13 at least one LSB integrator to generate integration
14 voltages on integration nodes by integrating charge associated
15 with the voltage of the input symbol [output] with respect to
16 the second and third threshold voltages; and

17 at least one LSB sense amplifier to receive the
18 integration voltages of the at least one LSB integrator to
19 generate at least one LSB logic signal representing [the] a
20 relationship of the input symbol to the second and third
21 threshold voltages,

22 wherein the I/O circuit stores signals representing the
23 MSB logic signal and the LSB logic signal in the subset of
24 memory cells of the memory array, as specified by the address.

1 23. (Amended) The memory of claim 20 wherein the MSB receiver
2 includes:

3 at least one MSB preamplifier to generate a MSB
4 preamplified signal in accordance with a relationship of the
5 input symbol to a first threshold voltage of the set of
6 threshold voltages;

7 at least one MSB integrator to accumulate charge to
8 produce an output voltage in accordance with the MSB
9 preamplified signal during an integration time interval

10 defined by a start integration timing event and an end
11 integration timing event; and
12 at least one MSB sense amplifier to sample and convert
13 the output voltage from the MSB integrator into a MSB logic
14 signal representing a [MSB] state of the the MSB of the input
15 signal; and
16 wherein the LSB receiver includes:

17 at least one LSB preamplifier to generate a LSB
18 preamplified signal in accordance with a relationship of the
19 input symbol to a second and third threshold voltage of the
20 set of threshold voltages;

21 at least one LSB integrator to accumulate charge to
22 produce an output voltage in accordance with the LSB
23 preamplified signal during an integration time interval
24 defined by a start integration timing event and an end
25 integration timing event; and

26 at least one LSB sense amplifier to sample and convert
27 the output voltage from the LSB integrator into an LSB logic
28 signal representing a [LSB] state of the LSB of the input
29 signal,

30 wherein the I/O circuit stores signals representing the
31 MSB logic signal and the LSB logic signal in the subset of
32 memory cells of the memory array, as specified by the address.

1 24. The memory of claim 23 wherein the first threshold
2 voltage is less than the second threshold voltage, and the
3 first threshold voltage is greater than the third threshold
4 voltage.

1 25. The memory of claim 20, further comprising:
2 a mode detection circuit to supply a PAM mode signal to
3 cause the MSB receiver and LSB receiver to operate in either
4 4-PAM or 2-PAM mode.

1 26. (Amended) A method [of correcting] for reducing errors in
2 a multi-Pulse Amplitude Modulated (PAM) system including a

3 multi-PAM output driver and a multi-PAM receiver coupled via a
4 data bus, comprising:

5 operating the multi-PAM output driver and the multi-PAM
6 receiver at 4-PAM to exchange multi-PAM data on a bus;

7 [determining whether] detecting an error [occurred] in
8 the multi-PAM data; and

9 operating the multi-PAM output driver and the multi-PAM
10 receiver at 2-PAM to exchange binary data on the bus in
11 response to detecting the error.

1 27. (Amended) The method of claim 26 wherein the multi-PAM
2 output driver and the multi-PAM receiver are operated at a
3 first [data] symbol rate, and further comprising:

4 reducing the first [data] symbol rate in response to
5 [the] further error detection.

1 28. (Amended) The method of claim 27 further comprising:

2 measuring an error-free time; and

3 increasing the first [data] symbol rate when the error-
4 free time equals a predetermined value.

1 29. The method of claim 27 further comprising:

2 measuring an error-free time; and

3 operating the multi-PAM output driver and the multi-PAM
4 receiver at 4-PAM when the error-free time equals a
5 predetermined value.

1 30. (Amended) A method [of correcting] for reducing errors in
2 a multi-Pulse Amplitude Modulated (PAM) system, comprising:

3 operating a multi-PAM output driver and a multi-PAM
4 receiver at 4-PAM to exchange data on a bus, the data having a
5 most-significant data bit and a least-significant data bit,
6 wherein the multi-PAM output driver and the multi-PAM receiver
7 transmit and receive an encoded multi-PAM symbol having a
8 most-significant symbol bit [(MSB)] and a least-significant
9 symbol bit [(LSB)], the most-significant data bit being

transmitted as the most-significant symbol bit, and the least-significant data bit being transmitted as the least-significant symbol bit;

[determining when] detecting an error [occurs] in the [data] multi-PAM symbol; and

[switching the MSB and LSB when an error occurs]
transmitting the least-significant data bit as the most-significant symbol bit and the most-significant data bit as the least-significant symbol bit in response to the error.

31. (Amended) A bus system comprising:

a signal line;

a first output driver to transmit a first data signal on the signal line;

a second output driver to transmit a second data signal on the signal line simultaneously with the first data signal such that the first and second data signals are superimposed to produce a superimposed data signal on the signal line, the superimposed data signal having a plurality of voltage levels representing the combinations of the simultaneously transmitted data signals;

a first receiver to receive the superimposed data signal, to determine a digital representation of the superimposed data signal, and [identifying] identify the data signal transmitted by the second output driver from the superimposed data signal; and

a second receiver to receive the superimposed data signal, to determine a digital representation of the superimposed data signal, and [identifying] identify the data signal transmitted from the first output driver from the superimposed data signal.

32. (Amended) A memory system comprising:

a bus having a plurality of signal lines [:] ;

a plurality of output drivers to drive an output symbol representing a predetermined number of bits including a most

5 significant bit (MSB) and a least significant bit (LSB) on a
6 first subset of the signal lines; and
7 a plurality of receivers, each receiver to receive the
8 output symbol from a respective signal line as an input
9 symbol, each input symbol representing the predetermined
10 number of bits, the receivers outputting a plurality of logic
11 signals representing the state of the MSB and LSB of the input
12 symbol.

1 33. The memory system of claim 32 wherein the memory system
2 is operated as a 4-PAM system such that the output symbol has
3 an MSB and an LSB; and the memory system is operated as a 2-
4 PAM system by setting the LSB of the output symbol to zero to
5 generate a 2-PAM symbol.

1 34. The memory system of claim 32 wherein the first set of
2 signal lines include control signal lines and data signal
3 lines, the control signal lines being 2-PAM, and the data
4 signal lines being 4-PAM.

1 35. The memory system of claim 32 wherein the memory system
2 is responsive to a mode signal to switch between 4-PAM and 2-
3 PAM.

1 36. The memory system of claim 35 wherein the mode signal is
2 determined by a hardware setting.

1 37. The memory system of claim 32 wherein the memory system
2 is responsive to detected errors to switch between 4-PAM and
3 2-PAM.

1 38. (Amended) A memory system comprising:
2 a bus having a plurality of signal lines;
3 a first subset of the signal lines being coupled to a
4 plurality of output drivers, each output driver to drive an
5 output symbol representing two bits including a most

6 significant bit (MSB) and a least significant bit (LSB) on the
7 signal line, each output driver including:

8 a first drive block to generate a MSB symbol
9 component representing the MSB; and

10 a second drive block to generate an LSB symbol
11 component representing the LSB, the LSB symbol component being
12 combined with the MSB symbol component to provide the output
13 symbol;

14 a second subset of the signal lines, including the first
15 subset of signal lines, being coupled to a plurality of bus
16 receivers to receive an address and [the output symbols, the
17 received output symbols being] input symbols, each input
18 symbol representing a predetermined number of bits, each bit
19 being associated with a distinct range of voltage levels, a
20 set of threshold voltages defining each distinct range of
21 voltage levels, each bus receiver including:

22 a most-significant bit (MSB) receiver to determine the
23 MSB of a respective one of the input symbols [symbol] based on
24 a first threshold voltage of the set of threshold voltages;
25 and

26 a least-significant bit (LSB) receiver to determine the
27 LSB of a respective one of the input symbols [symbol] based on
28 second and third threshold voltages of the set of threshold
29 voltages.

1 39. A method of operating a multi-drop bus using multi-level
2 signals, comprising:

3 transmitting an output symbol representing at least two
4 bits including a most significant bit (MSB) and a least
5 significant bit (LSB);

6 receiving the output symbol, the received output symbol
7 being an input symbol;

8 generating integration voltages by integrating charge on
9 at least one integration node in accordance with a state of
10 the input symbol; and

11 determining the MSB and the LSB in accordance with the
12 integration voltages.

1 40. An apparatus for transmitting data on a multi-drop bus
2 using multi-level signals, comprising:
3 means for transmitting an output symbol representing at
4 least two bits including a most significant bit (MSB) and a
5 least significant bit (LSB);
6 means for receiving the output symbol, the received
7 output symbol being an input symbol;
8 means for generating integration voltages by integrating
9 charge on at least one integration node in accordance with a
10 state of the input symbol; and
11 means for determining the MSB and the LSB in accordance
12 with the integration voltages.

NEW CLAIMS:

A10 1 41. (New) An apparatus for receiving multi-level signals, the
2 apparatus comprising:
3 a bus comprising a plurality of signal lines to carry
4 said multi-level signals comprising at least a first signal
5 and a second signal, said plurality of signal lines having at
6 least a first signal line and a second signal line carrying
7 said first signal and said second signal respectively, wherein
8 said multi-level signals have one of at least three (3)
9 distinct signal levels;
10 a plurality of multi-level receivers coupled to said
11 plurality of signal lines, said plurality of multi-level
12 receivers comprising a first multi-level receiver and a second
13 multi-level receiver, wherein said first multi-level receiver
14 is coupled to said first signal line to receive said first
15 signal and said second multi-level receiver is coupled to said
16 second signal line to receive said second signal;
17 said first multi-level receiver generating a first
18 output; and

19 said second multi-level receiver generating a second
20 output, wherein said first and second outputs collectively
21 represent more than two (2) digital bits.

1 42. (New) The apparatus of claim 41 wherein said bus is a
2 multi-drop bus.

1 43. (New) The apparatus of claim 42 wherein said multi-drop
2 bus is terminated.

1 44. (New) The apparatus of claim 41 wherein said plurality of
2 signal lines are terminated with a terminating resistor.

1 45. (New) The apparatus of claim 41 wherein said multi-level
2 signals have one of at least four (4) distinct levels.

1 46. (New) The apparatus of claim 41 wherein said at least
2 three distinct signal levels are voltage levels.

1 47. (New) The apparatus of claim 41 wherein said at least
2 three distinct signal levels are current levels.

1 48. (New) The apparatus of claim 41 wherein said first multi-
2 level receiver and said second multi-level receiver comprise a
3 first integrator and a second integrator respectively.

1 49. (New) The apparatus of claim 48 wherein said first multi-
2 level receiver comprises a first sampling circuit to sample
3 said first signal between transitions of said first signal.

1 50. (New) The apparatus of claim 49 wherein said second
2 multi-level receiver comprises a second sampling circuit to
3 sample said second signal between transitions of said second
4 signal.

1 51. (New) The apparatus of claim 50 wherein said first
2 sampling circuit and said second sampling circuit sample in
3 response to a clock transition.

1 52. (New) The apparatus of claim 41 wherein said first multi-
2 level receiver and said second multi-level receiver comprise a
3 first decoder and a second decoder, respectively, to decode
4 said first signal and said second signal on a clock
5 transition.

1 53. (New) The apparatus of claim 52 wherein said multi-level
2 signals collectively represent a data value.

1 54. (New) The apparatus of claim 52 wherein said multi-level
2 signals collectively represent a control value.

1 55. (New) The apparatus of claim 54 wherein said control
2 value represents an address.

1 56. (New) The apparatus of claim 54 wherein said control
2 value represents a read command.

1 57. (New) The apparatus of claim 54 wherein said control
2 value represents a write command.

1 58. (New) An apparatus for transmitting multi-level signals
2 comprising:
3 a bus comprising a plurality of signal lines to carry
4 said multi-level signals comprising at least a first signal
5 and a second signal, said plurality of signal lines having at
6 least a first signal line and a second signal line carrying
7 said first signal and said second signal respectively, wherein
8 said multi-level signals have one of at least three (3)
9 distinct signal levels; and
10 a plurality of multi-level output drivers coupled to said
11 plurality of signal lines, said plurality of multi-level

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12 output drivers comprising a first multi-level output driver
13 and a second multi-level output driver,
14 said first multi-level output driver outputting said
15 first signal onto said first signal line; and
16 said second multi-level output driver outputting said
17 second signal onto said second signal line, wherein said first
18 and second signals collectively represent more than two (2)
19 digital bits.

1 59. (New) The apparatus of claim 58 wherein said multi-level
2 signals have one of at least four (4) distinct levels.

1 60. (New) The apparatus of claim 58 wherein said at least
2 three distinct signal levels are voltage levels.

1 61. (New) The apparatus of claim 58 wherein said at least
2 three distinct signal levels are current levels.

1 62. (New) The apparatus of claim 58 wherein said plurality of
2 multi-level output drivers are current drivers.

1 63. (New) The apparatus of claim 58 wherein said multi-level
2 signals collectively represent a data value.

1 64. (New) The apparatus of claim 58 wherein said multi-level
2 signals collectively represent a control value.

1 65. (New) The apparatus of claim 64 wherein said control
2 value represents an address.

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4 66. (New) The apparatus of claim 64 wherein said control
5 value represents a read command.

1 67. (New) The apparatus of claim 64 wherein said control
2 value represents a write command.

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1 68. (New) A multi-level signaling system comprising:
2 a signaling path comprising a plurality of signal lines
3 including a first signal line and a second signal line;
4 a plurality of multi-level output drivers coupled to said
5 signaling path to output thereon multi-level signals
6 comprising at least a first signal and a second signal,
7 wherein said multi-level signals have one of at least three
8 (3) distinct signal levels;

9 said plurality of multi-level output drivers comprising a
10 first multi-level output driver and a second multi-level
11 output driver, wherein said first multi-level output driver
12 outputs said first signal onto said first signal line and said
13 second multi-level output driver outputs said second signal
14 onto said second signal line, wherein said first signal and
15 said second signal collectively represent more than two (2)
16 digital bits;

17 a plurality of multi-level receivers coupled to said
18 signaling path to receive therefrom said multi-level signals,
19 said plurality of multi-level receivers comprising a first
20 multi-level receiver and a second multi-level receiver,
21 wherein said first multi-level receiver is coupled to said
22 first signal line to receive said first signal and said second
23 multi-level receiver is coupled to said second signal line to
24 receive said second signal;

25 said first multi-level receiver generating a first
26 output; and

27 said second multi-level receiver generating a second
28 output, wherein said first output and said second output
29 collectively represent more than two (2) digital bits.

1 69. (New) The apparatus of claim 68 wherein said signaling
2 path is a multi-drop bus.

1 70. (New) The apparatus of claim 69 wherein said multi-drop
2 bus is terminated.

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1 71. (New) The apparatus of claim 68 wherein said plurality of
2 signal lines are terminated with a terminating resistor.

1 72. (New) The apparatus of claim 68 wherein said at least
2 three distinct signal levels are voltage levels.

1 73. (New) The apparatus of claim 68 wherein said at least
2 three distinct signal levels are current levels.

1 74. (New) The apparatus of claim 68 wherein said first multi-
2 level receiver and said second multi-level receiver comprise a
3 first integrator and a second integrator respectively.

1 75. (New) The apparatus of claim 74 wherein said first multi-
2 level receiver comprises a first sampling circuit to sample
3 said first signal between transitions of said first signal.

1 76. (New) The apparatus of claim 75 wherein said second
2 multi-level receiver comprises a second sampling circuit to
3 sample said second signal between transitions of said second
4 signal.

1 77. (New) The apparatus of claim 76 wherein said first
2 sampling circuit and said second sampling circuit sample in
3 response to a clock transition.

1 78. (New) The apparatus of claim 68 wherein said first multi-
2 level receiver and said second multi-level receiver comprise a
3 first decoder and a second decoder respectively to decode said
4 first signal and said second signal on a clock transition.

1 79. (New) The apparatus of claim 68 wherein said plurality of
2 multi-level output drivers are current drivers.

1 80. (New) A memory device comprising:
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3 a signaling path carrying multi-level signals comprising
4 at least a first signal and a second signal, said signaling
5 path comprising a plurality of signal lines including a first
6 signal line and a second signal line carrying said first
7 signal and said second signal respectively, wherein said
8 multi-level signals have one of at least three (3) distinct
9 signal levels, and said first signal and said second signal
10 collectively represent more than two (2) digital bits;

11 a plurality of multi-level receivers coupled to said
12 signaling path to receive therefrom said multi-level signals,
13 said plurality of multi-level receivers comprising a first
14 multi-level receiver and a second multi-level receiver,
15 wherein said first multi-level receiver is coupled to said
16 first signal line to receive said first signal and said second
17 multi-level receiver is coupled to said second signal line to
18 receive said second signal;

19 said first multi-level receiver and said second multi-
20 level receiver generating at least a first digital bit and a
21 second digital bit based on said first signal and said second
22 signal; and

23 an array of memory cells coupled to said plurality of
24 multi-level receiver circuits to store said first digital bit
25 and said second digital bit.

1 81. (New) The apparatus of claim 80 wherein said signaling
2 path is a multi-drop bus.

1 82. (New) The apparatus of claim 81 wherein said multi-drop
2 bus is terminated.

1 83. (New) The apparatus of claim 80 wherein said first multi-
2 level receiver and said second multi-level receiver comprise a
3 first integrator and a second integrator respectively.

1 84. (New) The apparatus of claim 83 wherein said first multi-
2 level receiver comprises a first sampling circuit to sample
3 said first signal between transitions of said first signal.

1 85. (New) The apparatus of claim 84 wherein said second
2 multi-level receiver comprises a second sampling circuit to
3 sample said second signal between transitions of said second
4 signal.

1 86. (New) The apparatus of claim 85 wherein said first
2 sampling circuit and said second sampling circuit sample in
3 response to a clock transition.

1 87. (New) The apparatus of claim 80 wherein said first multi-
2 level receiver and said second multi-level receiver comprise a
3 first decoder and a second decoder respectively to decode said
4 first signal and said second signal on a clock transition.

1 88. (New) A memory device comprising:
2 an array of memory cells;
3 a plurality of multi-level output drivers coupled to said
4 array of memory cells to receive a data value therefrom, said
5 data value comprising N bits, where N is an integer; and
6 said plurality of multi-level output drivers being
7 structured to output M signals representative of said data
8 value onto a signaling path where M is an integer less than
9 N, said M signals having one of at least three (3) distinct
10 signal levels.

1 89. (New) The apparatus of claim 88 wherein said at least
2 three distinct signal levels are voltage levels.

1 90. (New) The apparatus of claim 88 wherein said at least
2 three distinct signal levels are current levels.

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1 91. (New) The apparatus of claim 88 wherein said plurality of
2 multi-level output drivers are current drivers.

1 92. (New) The apparatus of claim 88 wherein said M signals
2 collectively represent a data value.

1 93. (New) The apparatus of claim 88 wherein said M signals
2 collectively represent a control value.

1 94. (New) A memory controller for transmitting M1 signals to
2 a memory device and receiving M2 signals from said memory
3 device, where said M1 and M2 are integers, said memory
4 controller comprising:

5 a plurality of multi-level output drivers to output to
6 said memory device said M1 signals representative of a first
7 data value comprising N1 bits, where N1 is an integer greater
8 than M1, said M1 signals having one of at least three distinct
9 signal levels; and

10 a plurality of multi-level receivers to receive from said
11 memory device said M2 signals representative of a second data
12 value comprising N2 bits, where N2 is an integer greater than
13 M2, said M2 signals having one of said at least three (3)
14 distinct signal levels.

1 95. (New) The apparatus of claim 94 wherein said plurality of
2 multi-level receivers comprise a plurality of integrators.

1 96. (New) The apparatus of claim 95 wherein said plurality of
2 multi-level receivers comprise a plurality of sampling
3 circuits to sample said M2 signals between transitions of said
4 M2 signals.

1 97. (New) The apparatus of claim 96 wherein said plurality of
2 sampling circuits sample in response to a clock transition.

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1 98. (New) The apparatus of claim 94 wherein said plurality of
2 multi-level receivers comprise a plurality of decoders to
3 decode said M2 signals.

1 99. (New) The apparatus of claim 94 wherein said plurality of
2 multi-level output drivers are current drivers.

1 100. (New) The apparatus of claim 94 wherein said at least
2 three distinct signal levels are voltage levels.

1 101. (New) The apparatus of claim 94 wherein said at least
2 three distinct signal levels are current levels.

410 Cont.
1 102. (New) A memory system comprising:
2 a signaling path;
3 a memory device having a plurality of multi-level output
4 drivers coupled to said signaling path to output thereon M
5 signals representative of a data value comprising N bits,
6 where M and N are integers and M is less than N, said M
7 signals having one of at least three (3) distinct signal
8 levels; and
9 a memory controller having a plurality of multi-level
10 receivers coupled to said signaling path to receive therefrom
11 said M signals, decode said M signals and produce an output
12 representative of said data value.

1 103. (New) The apparatus of claim 102 wherein said signaling
2 path is a multi-drop bus.

1 104. (New) The apparatus of claim 102 wherein said plurality
2 of multi-level receivers comprise a plurality of integrators.

1 105. (New) The apparatus of claim 104 wherein said plurality
2 of multi-level receivers comprise a plurality of sampling

3 circuits to sample said M signals between transitions of said
4 M signals.

1 106. (New) The apparatus of claim 105 wherein said plurality
2 of sampling circuits sample in response to a clock transition.

1 107. (New) The apparatus of claim 102 wherein said plurality
2 of multi-level receivers comprise a plurality of decoders to
3 decode said M signals.

1 108. (New) The apparatus of claim 107 wherein said multi-level
2 signals collectively represent a data value.

1 109. (New) The apparatus of claim 107 wherein said multi-level
2 signals collectively represent a control value.

1 110. (New) The apparatus of claim 102 wherein said at least
2 three distinct signal levels are voltage levels.

1 111. (New) The apparatus of claim 102 wherein said at least
2 three distinct signal levels are current levels.

1 112. (New) The apparatus of claim 102 wherein said plurality
2 of multi-level output drivers are current drivers.

REMARKS

Please enter the amendment After entry of this
amendment, the pending claims are: claims 1-112.

The change in the specification on page 84, line 12, is
to correct a typographical error.